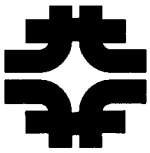

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The Use of Low Resistivity Substrates for Optimal Noise Reduction, Ground Referencing, and Current Conduction in Mixed Signal ASICs

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Fermilab, 11/97

INTRODUCTION

This paper is distilled from a talk given at the 3rd International Meeting on Front End Electronics in Taos, N.M. on Nov. 7,1997. It is based on experience gained by designing and testing the SVX3 128 channel silicon strip detector readout chip. The SVX3 chip organization is shown in Fig. 1. The Front End section consists of an integrator and analog pipeline designed at Fermilab, and the Back End section is an ADC plus sparsification and readout logic designed at LBL. SVX3 is a deadtimeless readout chip, which means that the front end is acquiring low level analog signals while the back end is digitizing and reading out digital signals. It is thus a true mixed signal chip, and demands close attention to avoid disastrous coupling from the digital to the analog sections.

SVX3 is designed in a bulk CMOS process (i.e., the circuits sit in a silicon substrate). In such a process, the substrate becomes a potential coupling path. This paper discusses the effect of the substrate resistivity on coupling, and also goes into a more general discussion of grounding and referencing in mixed signal designs and how low resistivity substrates can be used to advantage. Finally, an alternative power supply current conduction method for ASICs is presented as an additional advantage which can be obtained with low resistivity substrates.

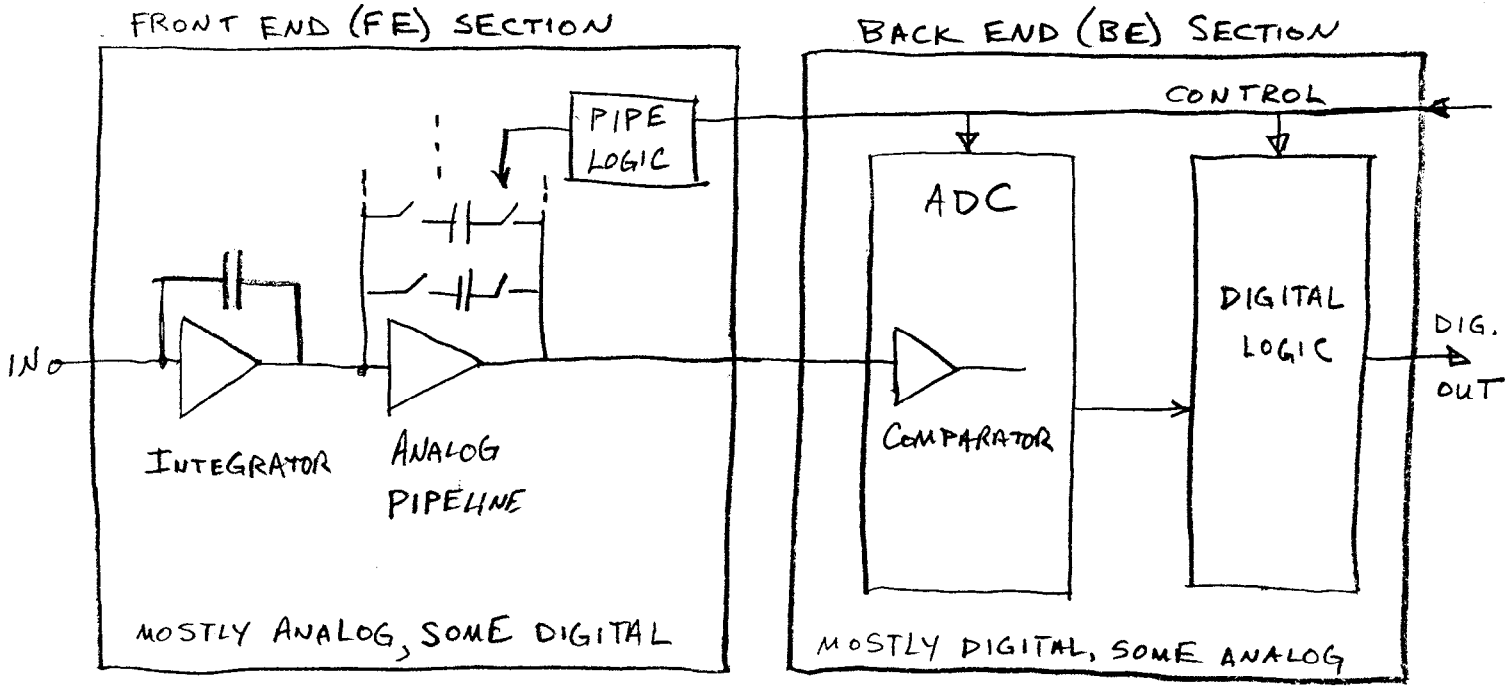


Fig. 1. Simplified SVX3 block diagram.

NOISE COUPLING AND REFERENCING PROBLEMS

Noise coupling and supply referencing are important issues in mixed signal ASIC design! In some cases, problems are purely internal to the chip, e.g., trace to trace capacitive coupling or common impedance coupling. Often these problems can be controlled by proper design and layout. In other cases, problems may be external to the chip, e.g., capacitive and inductive coupling through bondwires and PC traces, common impedance coupling due to finite reference impedance, and ground, power, and bypassing inadequacies. All too often, these "external" issues are not considered when doing the chip design.

At the interface of the two worlds are two important issues: substrate coupling and ground/power referencing problems. These problems are affected by both chip layout philosophy **and** the external (PC board or hybrid) layout and connection philosophy. It is important to consider **both** philosophies during the chip design phase.

Substrate coupling problems are typically caused by a noisy digital supply coupling to the substrate through a large parasitic capacitance, infecting the substrate in analog parts of the chip.

Referencing problems are typically caused by current transients flowing through a non-zero impedance reference (such as ground or power), causing non-identical reference voltages for different circuits.

Modern bulk CMOS processes (usually p substrate, N-well) have one of two types of substrates:

1. High resistivity (p-)

2. Low resistivity (p+), with a thin epitaxial p- layer deposited on top where the actual circuits are formed.

The chip substrate resistivity will have a big effect on noise coupling properties on-chip. The substrate resistivity thus plays a big part in determining the optimal noise reduction and grounding philosophy.

GROUNDING AND REFERENCING IN MIXED SIGNAL CHIPS

Before investigating how the chip substrate affects coupling, it is worthwhile to take an aside about a more general topic, that of grounding and referencing. This is a huge topic, which certainly cannot be covered comprehensively. However, there are a few important general principles which apply to mixed signal chip design which should be emphasized here. Correctly applying these principles to the SVX3 chip design, in tandem with exploiting the properties of low resistivity substrates, proved to be crucial in obtaining the best performance from the SVX3 chip.

First, what exactly is the ground? There is of course no magic absolute ground -- it's all relative. Each of many different circuits on a chip may have a reference node, or ground. All ground nodes must ultimately be brought out (separately or combined in some way) and connected to a distrib-

uted external "system ground" node. This reference node is commonly a "ground plane." A plane structure conveniently distributes the system ground for connection to all the circuit grounds, and importantly, has inherently low impedance. Ideally, a distributed ground node should have zero impedance, so that voltage differences cannot develop across it in the presence of current transients. To be most effective, all points on the plane must be at the same potential. This is especially important when analog circuits are involved. For example, if there is a non-zero AC potential between the references ("grounds") of two analog sections on a chip, then that AC potential is effectively a noise voltage between the two circuits. Digital circuits are more able to tolerate non-identical references, as long as the effective "noise voltage" is less than the digital noise margin.

Since mixed signal designs contain both sensitive analog circuits and digital circuits (with their attendant large supply current transients), there is a well founded natural concern that digital activities will corrupt analog circuitry. An important question is: **How do we keep the references clean in a mixed signal ASIC, so that the operation of one circuit does not affect the reference of another circuit?**

Inevitably, all circuit reference connections have some finite impedance. For example, the ground of any circuit on a chip must be bussed with finite resistance metal, typically to a bond pad. A bond wire connection to an external ground plane is then supplied which has some resistance and a significant inductance. Impedance in the reference of a given circuit is not necessarily disastrous. In fact, many circuits by themselves can tolerate substantial ground impedance. A much more serious problem is the **sharing of a common impedance** by the references of two different circuits. In this case, operation of one circuit can cause a significant unintended noise on the reference of another circuit.

In order to avoid this common impedance coupling problem, mixed signal chips usually have the analog power and ground connections separated from the digital power and ground. In fact, several separate supply connections may be necessary within the analog section alone to eliminate low levels of common impedance coupling between analog subsections. Sharing a common bond wire between analog and digital sections, as shown in Fig. 2a, would be disastrous due to the voltage developed by the digital current. The necessity of separating the analog and digital grounds at the chip level leads to the natural inclination to extend the concept by having separate analog and digital ground planes for the chip as shown in Fig. 2b. This seems like a logical approach, since noisy circuits would be connected only to the digital ground plane, and quiet circuits to the analog plane. However, this is an erroneous conclusion. Separate analog and digital grounds means that there is a relatively high impedance (at least at high frequencies) between the two grounds. Higher impedance leads to larger noise voltages being developed on the digital ground with respect to the analog ground. Since the digital and analog circuits are in relatively close proximity on the same die, and the digital circuits may actually perform controlling functions on the analog circuits, there is inevitable parasitic capacitance between the digital power/ground and the analog circuitry. Thus digital power/ground excursions can couple significantly to the analog circuits. This makes it important to **minimize** the impedance between analog and digital grounds on a chip, while still minimizing common impedance coupling between the two. The best compromise between these two conflicting restraints is as shown in Fig. 2c, where the analog and digital chip grounds are connected directly to one "analog" system ground plane.

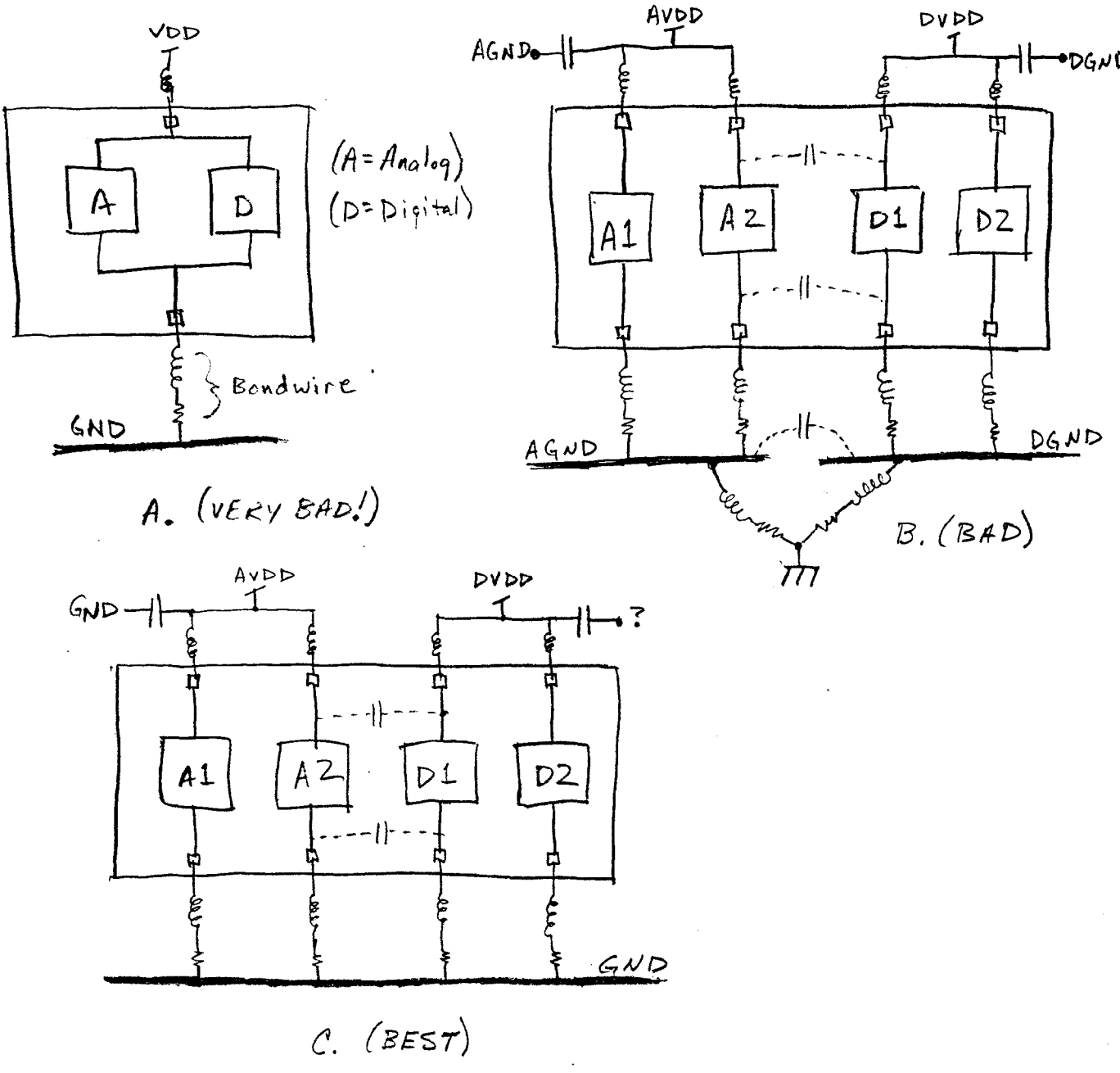


Fig. 2. Mixed signal chip grounding options.

At the system level, separate "analog" and "digital" ground planes may still be desirable. For example, the mixed signal chip may feed another chip some distance away which is purely digital and quite noisy. The digital chip could be referenced to a separate digital ground so that its transients will not affect the analog ground of the mixed signal chip. Noise voltage between the grounds is acceptable as long as it is less than the digital noise margin and does not couple to the mixed signal chip.

Or, as in the case of SVX3 chips and detectors, there may be many identical mixed signal chips in a large system which cannot all be practically connected to one ground plane. Since each detector with its several SVX3 chips can be considered as an isolated "mini-system" with a digital output, it is important to maintain one solid analog ground for each mini-system. At the digital level, the mini-system grounds can then be allowed to be somewhat separate from each other. See Fig. 3.

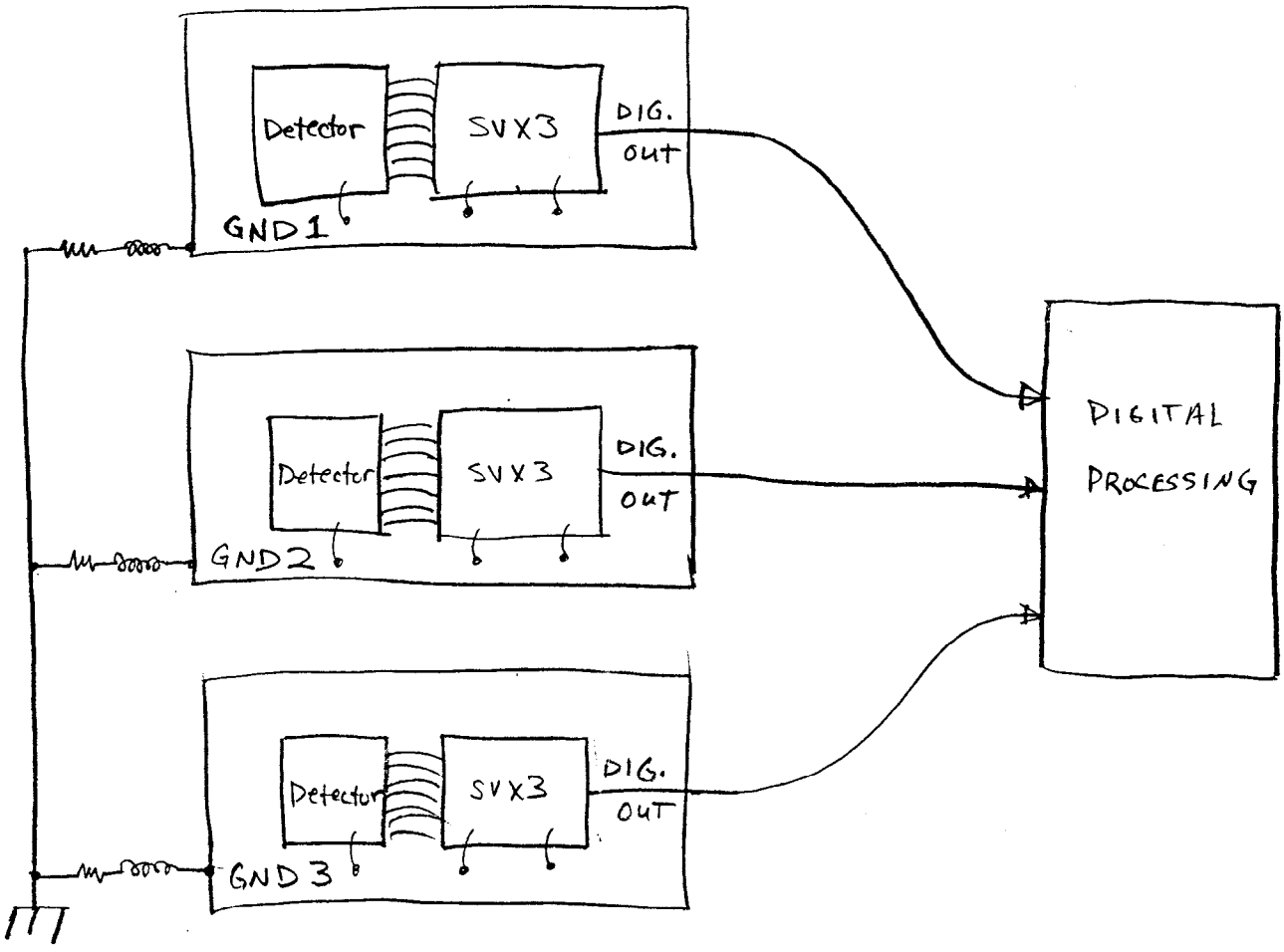
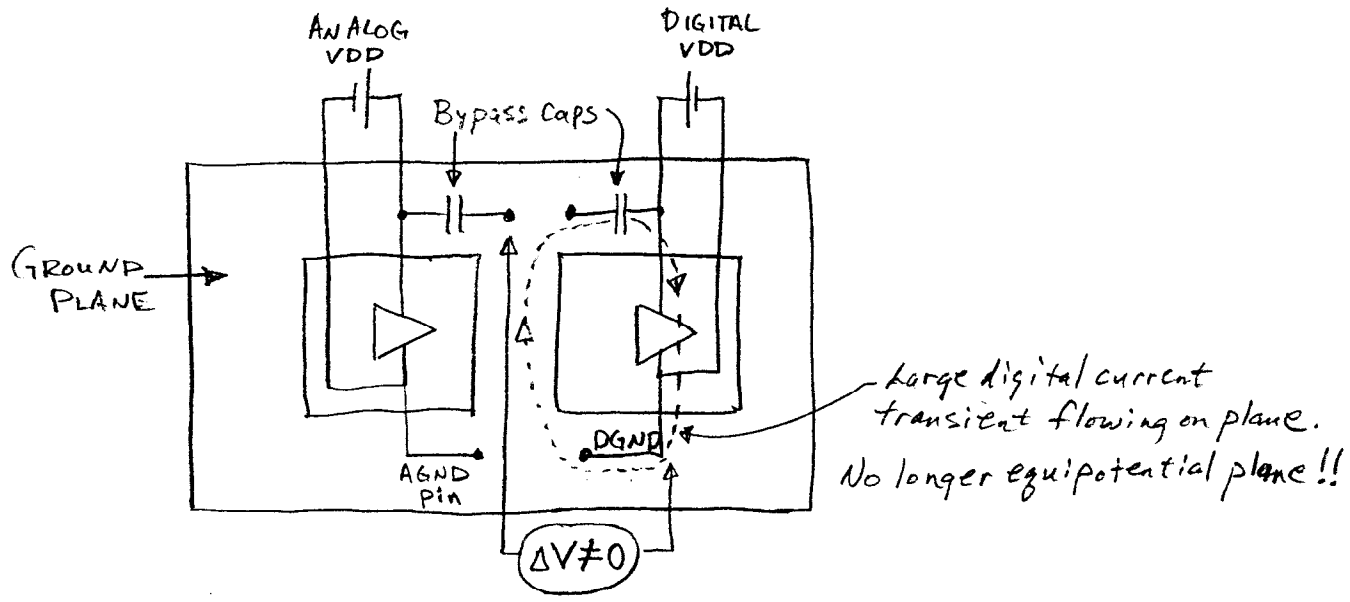
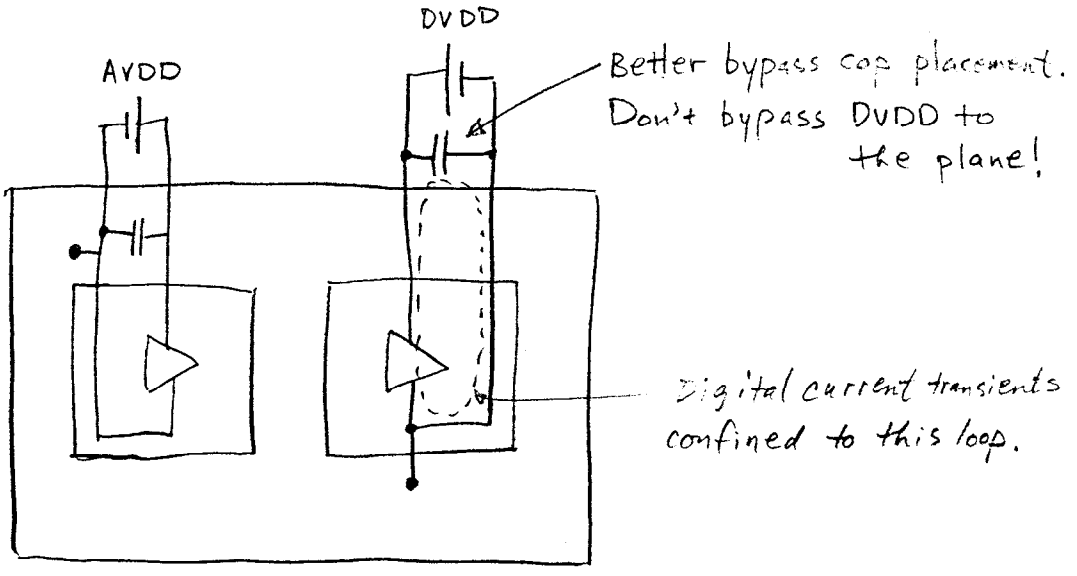


Fig. 3. Multi-chip system grounding.

Although adopting the "one ground" approach for mixed signal chips is the best grounding compromise, success is not automatically guaranteed. There are still potential pitfalls. For example, note the question in Fig. 2c as to where to connect the digital supply bypass capacitor. Fig. 4a shows the digital ground connected to the ground plane, and the digital supply bypassed to the plane some distance away. Since large digital current transients will flow through the plane, and the plane's impedance is low but still finite, noise voltages can be developed across the plane. These can easily couple into the analog circuits. In order to avoid this situation, it is important to keep current transients **off** of the plane! Fig. 4b shows a bypassing configuration which achieves this goal. The digital ground is still connected directly to the ground plane, but the bypassing is done in the supply loop so that the transients do not flow on the plane. This approach was demonstrated to be superior for SVX3, and should apply to mixed signal chips in general.



A. Digital transient current flowing through ground plane. **(BAD)**



B. Digital transients isolated from ground plane. **(BEST)**

Fig. 4. Digital bypass capacitor placement.

SUBSTRATE RESISTIVITY EFFECTS ON COUPLING

Even if all common impedance and referencing problems are eliminated in a mixed signal design, the analog and digital circuits still sit in the same silicon substrate (this does not apply to SOI processes, of course). N+ contacts or N wells which sit in a P substrate are effectively back biased diodes. Thus any voltage excursion on a contact or well couples capacitively to the substrate. Since the substrate has some finite resistivity, and is connected through some finite impedance to the system ground, the substrate presents a coupling path between circuits. An important question is: **If a noise voltage is injected onto the chip substrate in one location by a "noisy" circuit, what noise voltage is seen on the substrate at other locations around the chip?**

Fig. 5, excerpted from the *IEEE J. Solid-State Circuits*, models this situation with two contacts sitting in the same substrate some variable distance apart. The back-plane (substrate) of the chip is connected to system ground through a back-plane inductance L_{gnd}. A signal is applied to one of the contacts, and the coupling to the other contact is observed. The results are shown in Fig. 6 for high resistivity substrates and for low resistivity substrates. As can be seen, the behavior is very different for the two cases. Following is a summary of the properties for each case.

High resistivity substrate:

Substrate current has a significant horizontal component (i.e., mostly surface current).

Isolation is very dependent on distance. Larger distance = better isolation.

Isolation is a very weak function of the back-plane inductance.

Guard rings can be effective in improving isolation, since they shunt away surface noise currents.

Noise can be different at different location on the substrate, and is very dependent on geometry.

Low resistivity substrate:

Substrate current is mostly vertical (i.e., to the back-plane).

Beyond a small critical distance (25-50 microns), there is no improvement in isolation with distance.

Isolation is a strong function of back-plane inductance. Lower inductance = better isolation.

Guard rings are not effective, since noise currents are vertical.

The substrate noise is essentially the same over the complete substrate area, and independent of geometry.

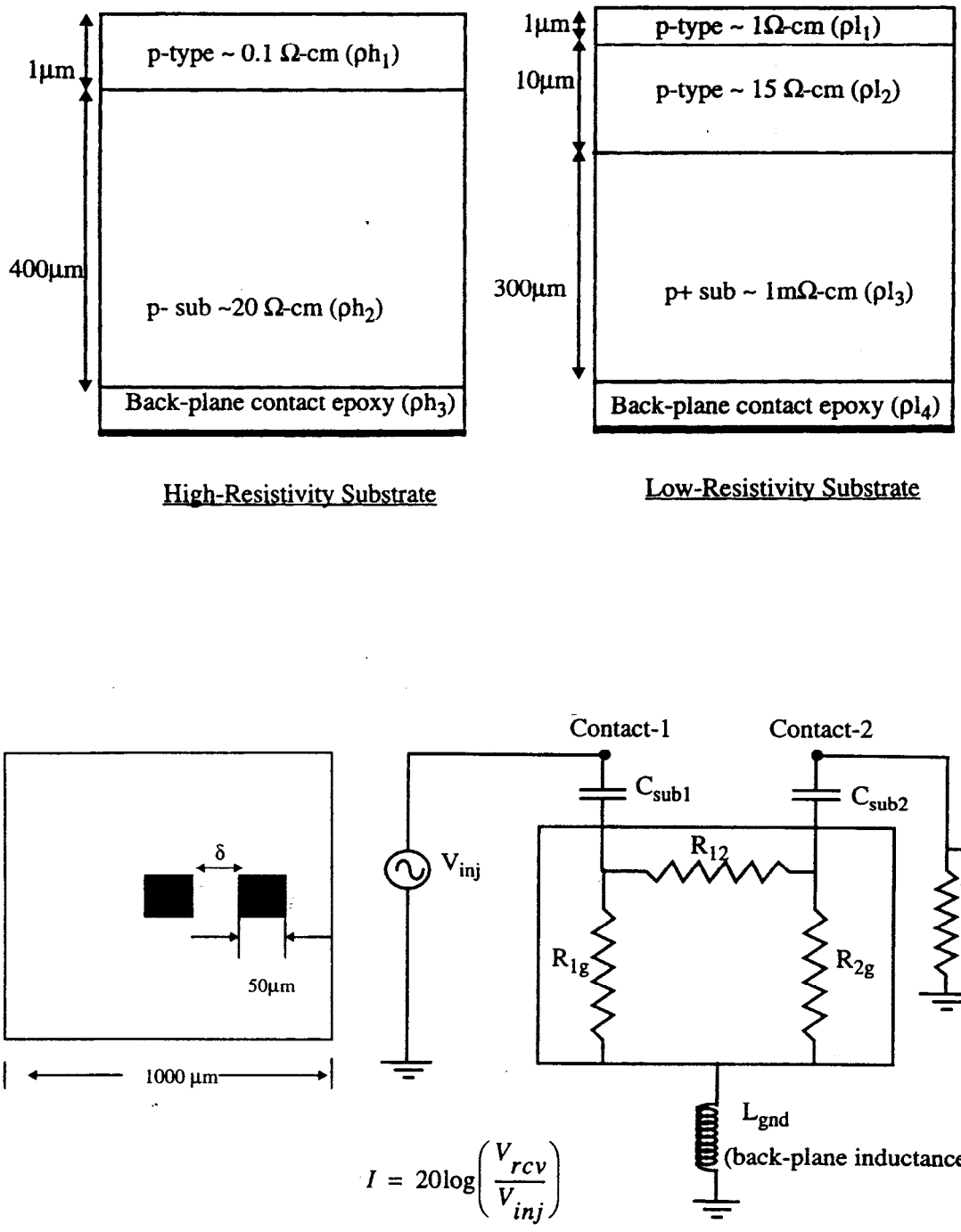
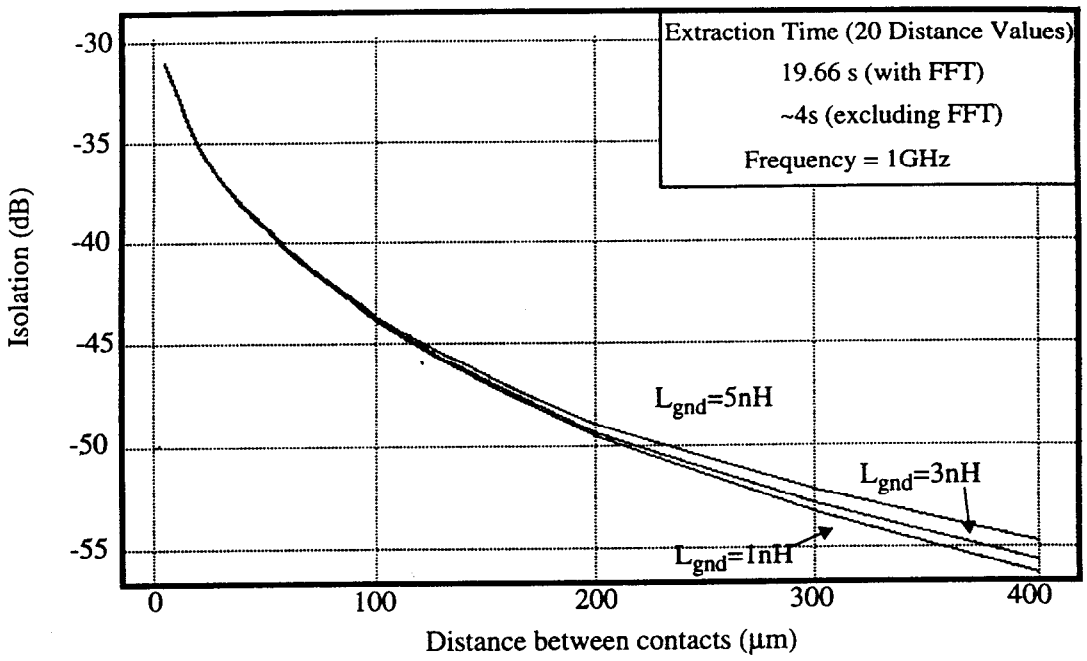
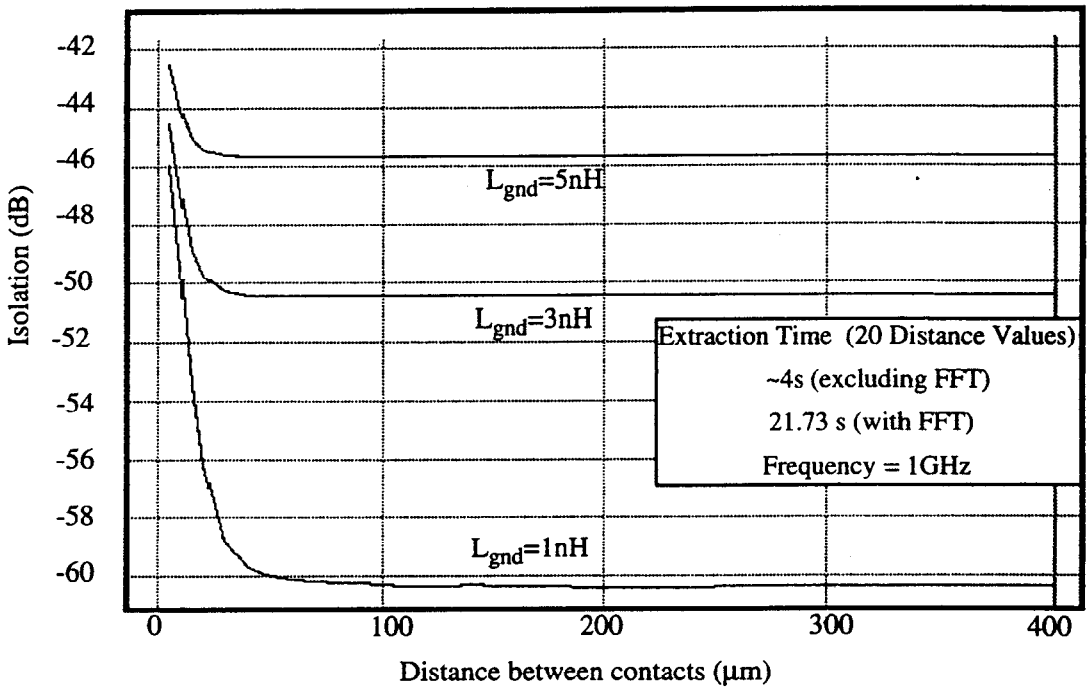


Fig. 5. Modeling of substrate coupling.

Reference: R. Gharpurey and R. Meyer, "Modeling and Analysis of Substrate Couping in Integrated Circuits," *IEEE J. Solid-State Circuits*, vol. 31, pp. 344-353, March 1996.



A. High resistivity substrate.



B. Low resistivity substrate.

Fig. 6. Isolation properties of substrates.

Reference: R. Gharpurey and R. Meyer, "Modeling and Analysis of Substrate Couping in Integrated Circuits," *IEEE J. Solid-State Circuits*, vol. 31, pp. 344-353, March 1996.

The conclusion which seems most obvious is that low resistivity substrates present the worst situation for substrate coupling. Any noise which couples to a low resistivity substrate in one location is essentially conducted to the back side of the chip and is spread over the whole substrate. With a high resistivity substrate, guard rings and distance can be used to improve isolation and reduce coupling from noisy to sensitive areas of the chip.

This conclusion is based on the assumption that L_{gnd} is several nH or more. This is usually a reasonable assumption, since a bondwire presents an inductance of about 20 nH/inch. It is difficult to reduce the bondwire plus package lead inductance to below a few nH. Most applications generally involve packaged chips, so Lgnd is unavoidable.

What happens to the isolation properties if L_{gnd} approaches zero? If the substrate is high resistivity, there is little effect. However, if the substrate is low resistivity, there is a **big** effect, as is suggested by Fig. 6. If the chip substrate can be attached directly to the system ground plane, the substrate effectively becomes just an extension of the reference ground plane, and the substrate coupling approaches zero! This is close to the ideal situation.

In some applications, it is possible to use unpackaged chips which are directly attached to the system ground. As an example, the SVX3 chip in fact cannot be packaged due to space and mass constraints. It must be attached directly to a hybrid ("chip on board"), then wire bonded directly to a detector. If it is glued with conductive epoxy directly to the hybrid ground, Lgnd then becomes **much** smaller than any bondwire inductance.

Many modern bulk CMOS processes, such as the H.P. 0.8u used for prototyping SVX3 and the Honeywell radiation hard 0.8u used for SVX3 production, use the low resistivity substrate structure. **Low resistivity substrates have attractive properties which can be exploited for significant noise reduction if unpackaged chips can be directly attached to system ground.**

OTHER ADVANTAGES OF LOW RESISTIVITY SUBSTRATES

As shown, attaching the back side of a chip with a low resistivity substrate directly to system ground can serve to practically eliminate substrate coupling. There are also other advantages that can be gained when using this method.

Chip substrates (p type) must be reverse biased at the lowest circuit potential so that there is no DC substrate current and to guard against latchup. In conventional practice, topside substrate contacts are distributed throughout chip layouts and connected to ground to insure that no portion of the substrate can become forward biased at any time. With low resistivity substrates, latchup protection is sufficient when using only the back side contact to bias the substrate. Top side contacts for latchup protection can then be eliminated, allowing higher layout packing density.

With conventional methods of supplying power to the circuits on a chip, the highly doped (p+) portion of the substrate serves mostly as a physical support for the epitaxial layer and as a vehicle through which to apply the reverse bias. However, since a highly doped substrate is inherently low resistance, it can actually be used to advantage as the power supply ground current conduction

path for analog circuits.

Fig. 7 shows the "conventional" supply current conduction method applied to the SVX3 chip. This familiar method works for low or high resistivity substrates. Wide metal busses route the Vdd and ground currents to bond pads, which are connected via bond wires to the external supplies. A back side contact is not necessarily required.

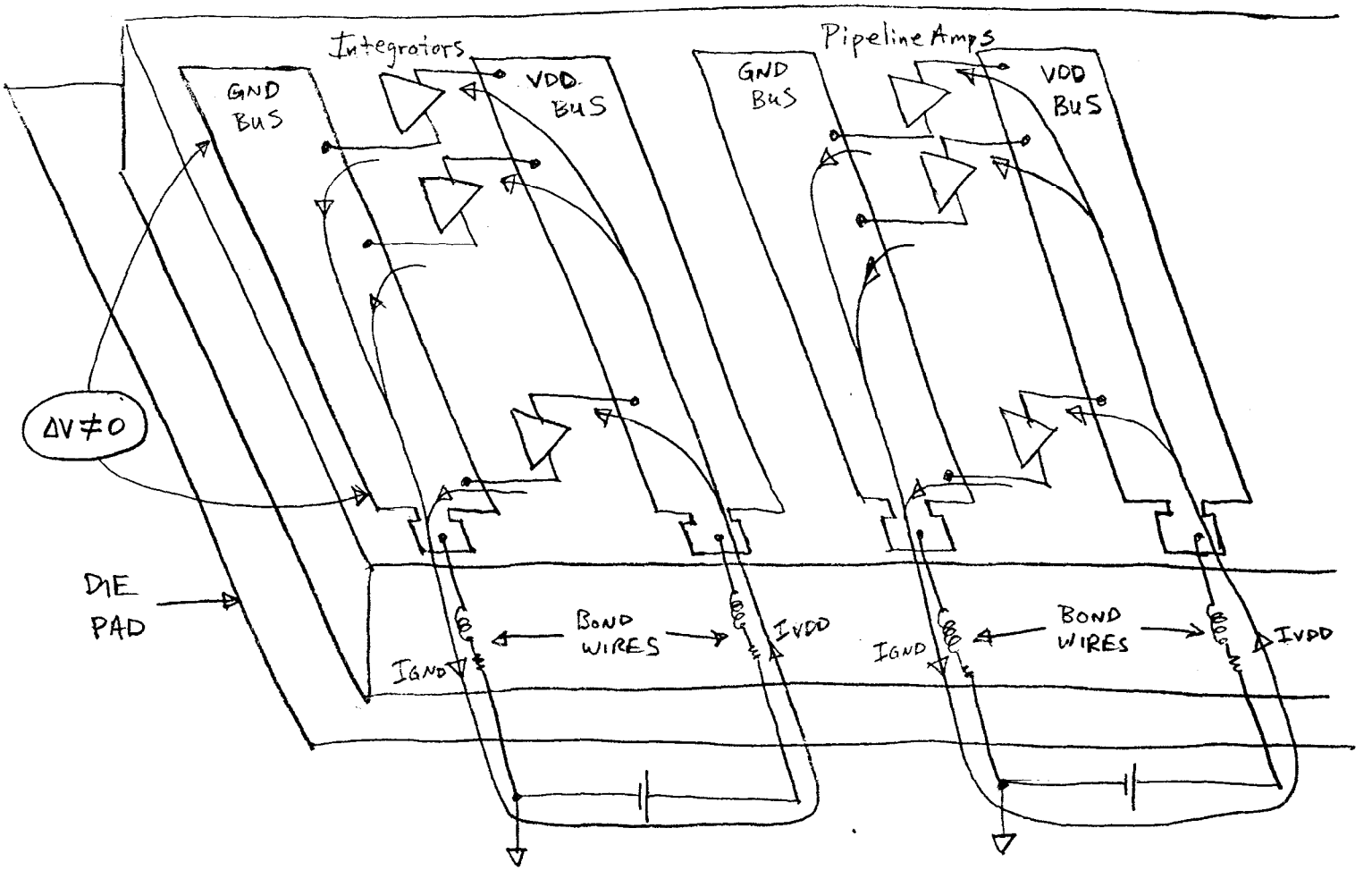


Fig. 7. Conventional supply current conduction method.

Fig. 8 illustrates the **substrate conduction** method, where the substrate serves as the conduction path for the ground current. This method requires a low resistivity substrate and a back side contact connected to system ground. Instead of a ground bus to a bond pad, a distributed substrate diffusion contact area is used to provide low resistance to ground through the back side and conduct the analog ground currents directly to the system ground plane. Note that the digital circuits are still supplied in the conventional manner, in order to keep large transient currents off of the ground plane, as discussed in the previous section.

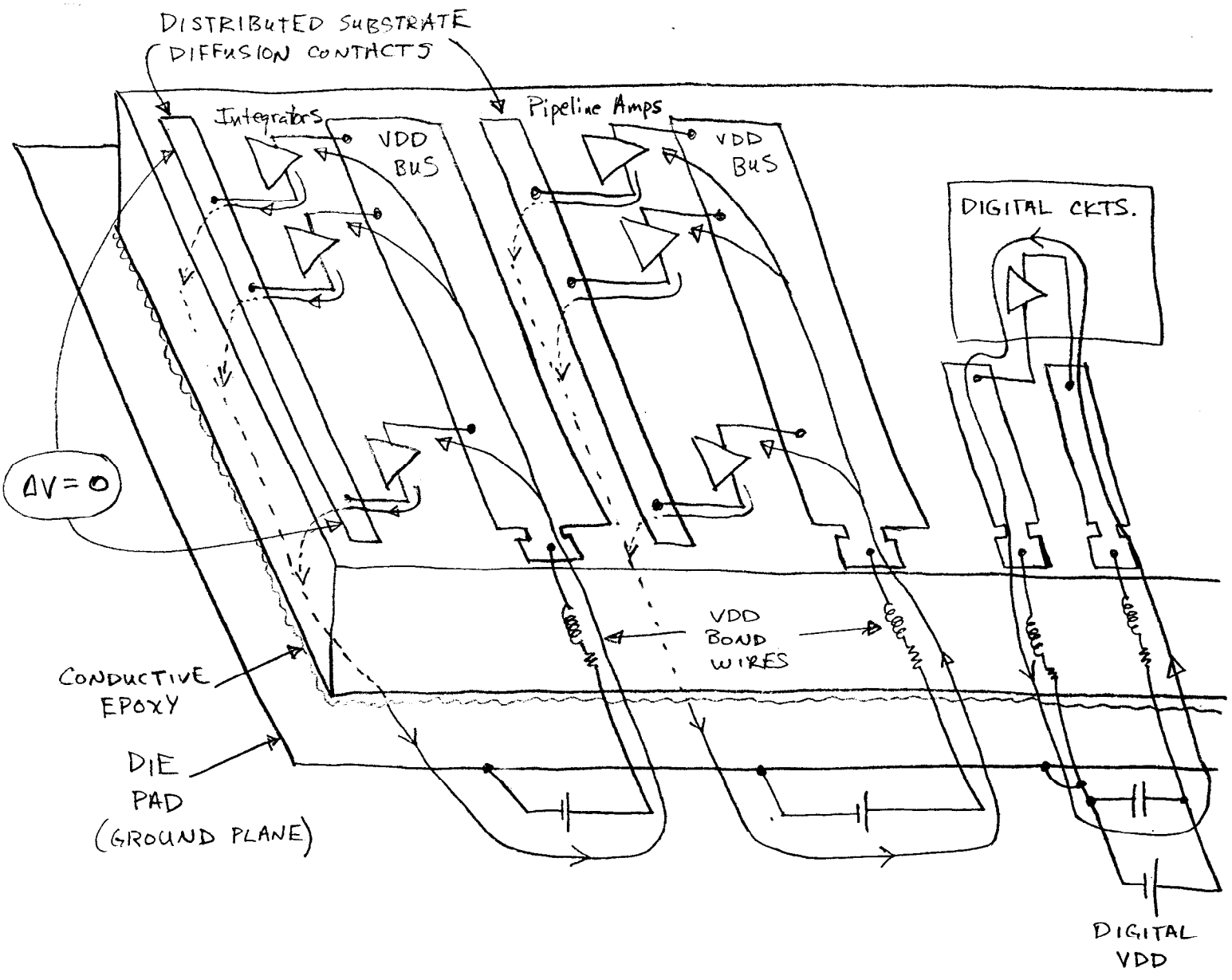


Fig. 8. Substrate conduction method for conducting supply current.

The major advantages of the substrate conduction method are:

1). Lower pad count (ground pads for the analog circuits are eliminated).

2). Low analog ground resistance. The resistance obtained is inversely proportional to the substrate diffusion bar area. For SVX3, a 5500u X 85u diffusion contact area yields a total ground resistance of less than 0.5 ohms, which is less than the conventional ground bus plus bond wire resistance.

3). Very low ground inductance (much lower than typical bond wire inductance).

4). All analog circuits using this grounding method will be intimately referenced directly to the system ground.

5). Less metal bussing area is required on the chip since the wide analog ground busses are eliminated. However, note that some extra chip area is required for substrate diffusion ground contact bars.

6). There is no ground bus voltage difference across the channels on a chip -- each channel on a multi-channel chip sees equal "ground" voltage since the ground current is distributed uniformly across the chip through the substrate diffusion bar.

OTHER CONSIDERATIONS IN REDUCING NOISE SENSITIVITY

The substrate referencing/conduction method has definite noise reduction advantages, but this does not mean that all noise problems will be automatically solved. Close attention must still be paid to other coupling paths, and to sensitivity to power supply noise. In order to use substrate referencing to full advantage, the most sensitive supply nodes of analog circuits should be ground (substrate), if possible. As an example of a potential noise sensitivity problem, the first SVX3 prototypes use a front end integrator as shown in Fig. 9. This is a folded cascode configuration with a PMOS input transistor. The integrator input node is the PMOS gate, and the input reference node is effectively the PMOS source, which is connected to an external supply, AVDD2. There is a parasitic capacitance C_p = 4 pF from the input to the substrate due to the input pad and trace. The integration (feedback) capacitance C_{fb} is 0.2 pF. In this configuration, the sensitivity of Vout to AVDD2 is Vout/AVDD2 ~ $(C_{det} + C_p)/C_{fb}$ = 25. Since the input capacitance is referred to substrate and not the reference node of the input transistor, Vout is very sensitive to fluctuations on AVDD2! In fact, the AVDD2 noise must be kept well below 0.1 mV in order be below the inherent integrator noise. This places very stringent demands on the AVDD2 supply, and would most likely be a significant source of unexpected noise in a final system.

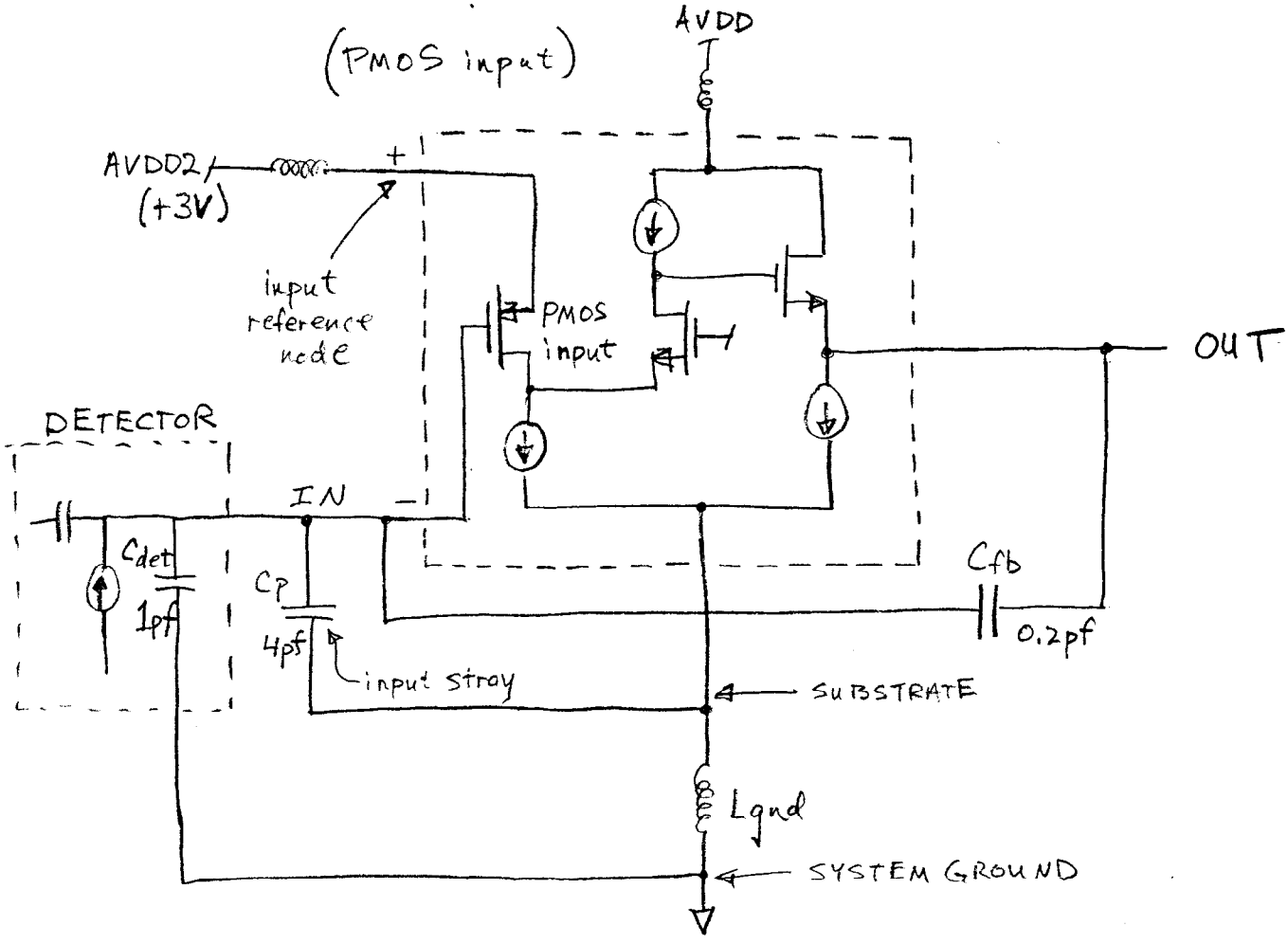


Fig. 9. SVX3 integrator with PMOS input.

In order to use the substrate properties to full advantage, the integrator configuration can be changed to that shown in Fig. 10. An NMOS input transistor is used so that the integrator input reference node is now just the substrate, or ground. This is a big improvement over the previous configuration, for two reasons:

1). Since the input parasitic capacitance is now between the input and the input reference node, the output sensitivity to the input reference node is greatly reduced (Vout/Vground ~ 1).

2). The input reference node is no longer referred to a power supply, but to substrate/ground, which is inherently quiet.

Thus, if possible, the gain element of an analog amplifier should be referenced to ground through the substrate.

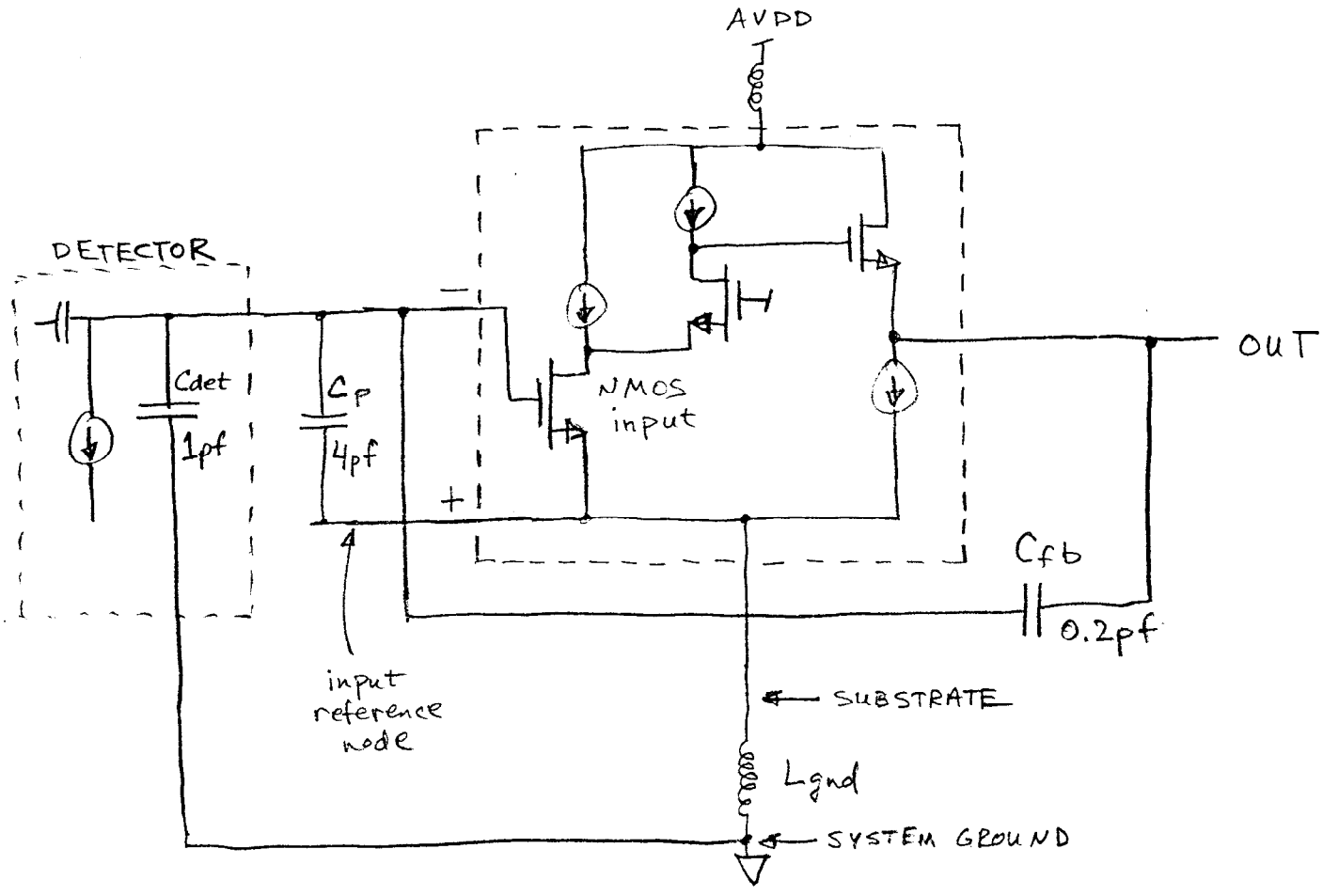


Fig. 10. SVX3 integrator with NMOS input.

TEST RESULTS

Substrate coupling tests were performed on SVX3 chips using different top side "ground contact" substrate diffusion bars which are spaced at intervals across the chip and used for ground current conduction. See Fig. 12. First, a chip was tested as received directly from the Honeywell foundry. The Honeywell chips come with a gold back side contact already applied as part of the fabrication process. Measurements show that the contacts can be crudely modeled by the circuit shown in Fig. 13. Each substrate diffusion bar has some finite resistance to the p+ bulk, as expected, but there is also a 0.65 ohm resistance between the bulk and the gold contact, with a parallel 0.17 uF capacitance. It is believed that there is some very thin oxide over a significant area of the bulk between the bulk and the gold contact, which causes a noticeable resistance with parallel capacitance.

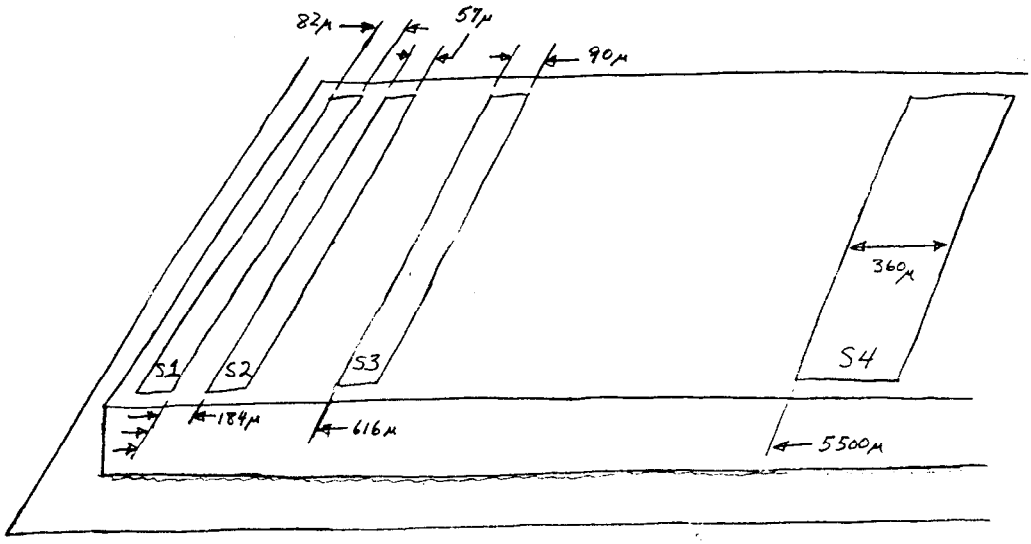


Fig. 11. SVX3 substrate diffusion contact bar layout.

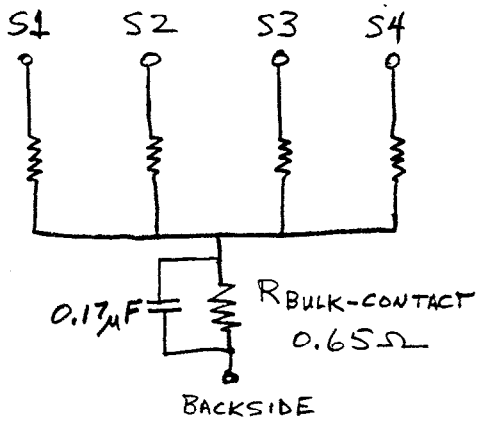


Fig. 12. Honeywell SVX3 substrate contact model (simplified).

A Honeywell wafer was sent out for backgrinding and backplating (all oxide is carefully removed before plating). The bulk-contact resistance was then measured to be < 0.0002 ohms! **Therefore, for best results, backgrind and backplate chips!** All subsequent test results are for chips which were background and plated.

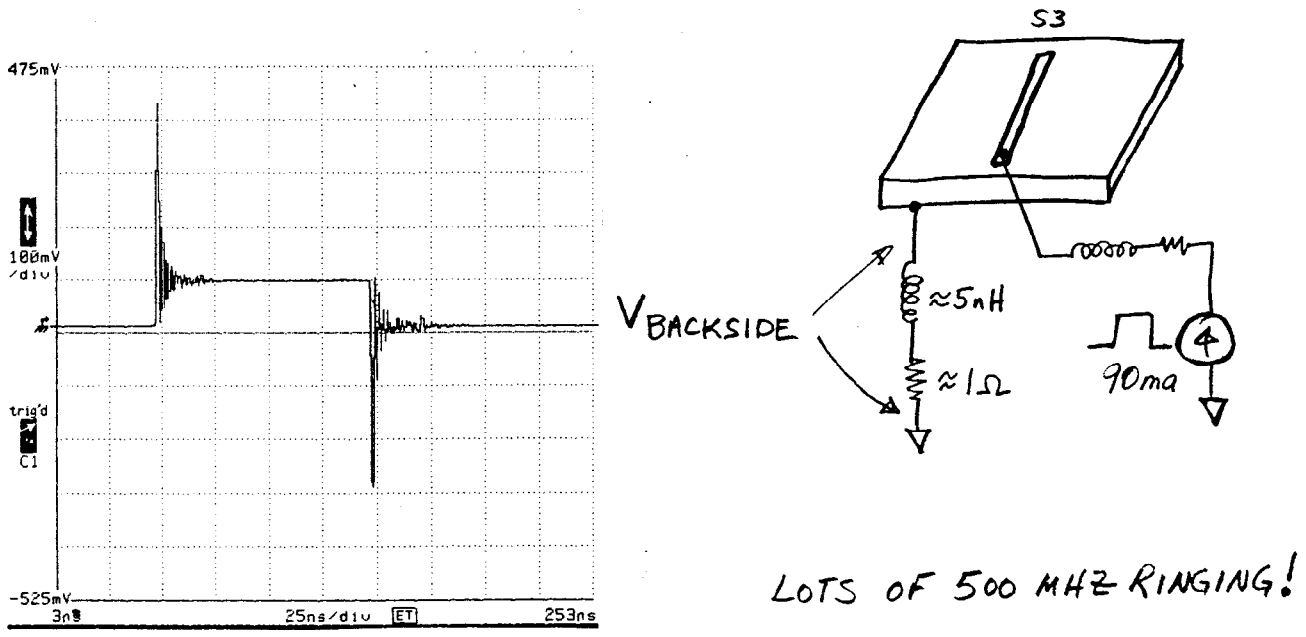
A DC power conduction test was performed to measure the coupling of a large DC current through one substrate diffusion contact bar to the other contacts. 100 mA was applied to the S1 contact, and voltages measured at the other contacts. The results are shown in Table 1.

Table 1:

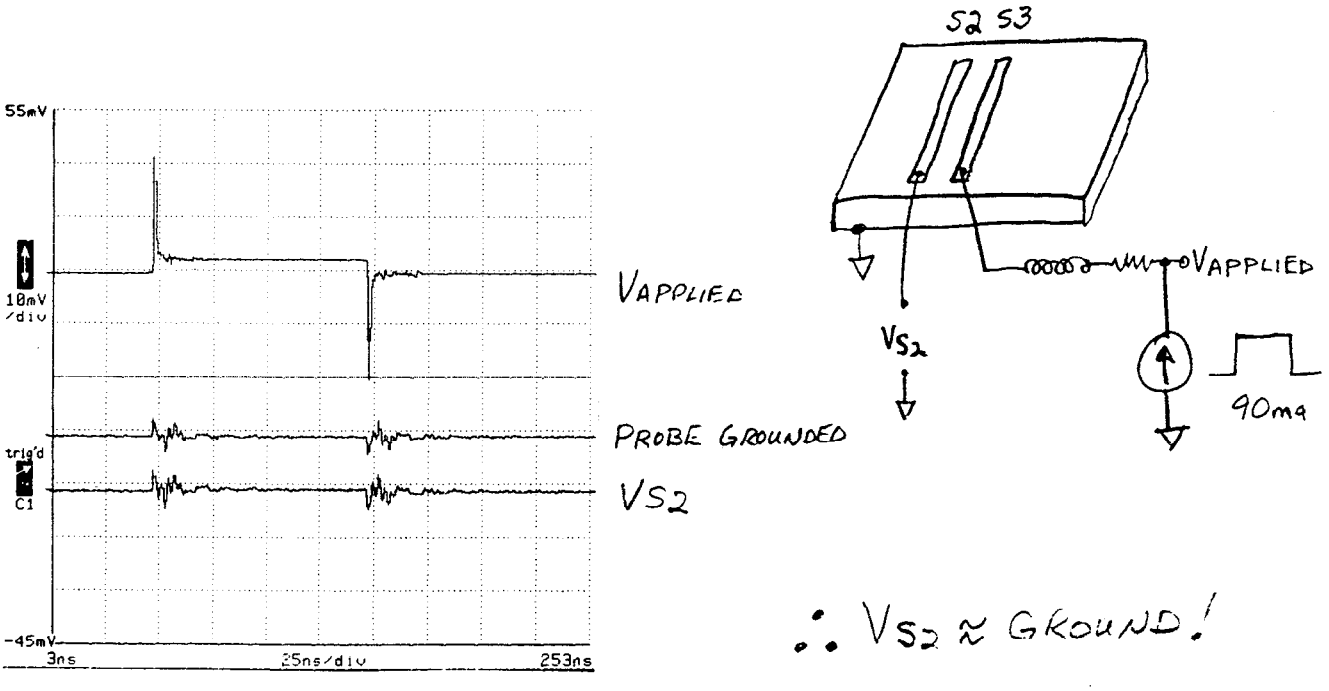
Substrate Contact Bar	Distance from S1	Measured Voltage
S1	--	47 mV
S2	184u	3.7 mV
S3	616u	0.58 mV
S4	5500u	0.02 mV

The S1 contact has a resistance of 0.47 ohms to the backplane, and so develops 47 mV. This would be the "ground" voltage of an analog circuit which draws 100 mA supply current. This could be decreased by increasing the diffusion contact area. The other contacts are not conducting any current, but pick up some small voltage since the current through S1 does not flow exactly vertically to the back plane, but spreads out slightly. Even at contact bar S2, which is relatively close to S1, the coupling from a 100 mA current through S1 is at the few mV level, which is small enough that it would not affect biasing of other analog circuits. For larger distances, the coupling is essentially zero.

The effectiveness of connecting the back side directly to ground in eliminating AC substrate coupling was demonstrated by applying a fast 90 mA current pulse under two different conditions: 1) chip back side connected to system ground through approximately 5 nH (bond wire), and 2) chip back side connected directly to system ground with conductive epoxy. The first situation is shown in Fig. 13a, where the current pulse is applied to the S3 substrate diffusion bar. The voltage observed on the substrate exhibits severe 500 MHz ringing (at the several hundred mV level) in addition to a step voltage due to the bondwire resistance. The second situation is shown in Fig. 13b. The pulse is again applied to S3, and the voltage on the substrate is measured several hundred microns away from S3 by looking at the S2 contact. High frequency ringing of a few mV is seen, however, approximately the same waveform is seen if the probe is just grounded! The noise voltage seen is just the magnetic pickup of the small probe loop. Therefore, for a 90 mA current transient through the substrate to the back side and system ground, the noise voltage seen at other points around the substrate is below the 1 mV level. In other words, the isolation is excellent!



A. Inductive backside connection.



B. Back side directly to ground plane ($L_{gnd} \sim 0$).

Fig. 13. Substrate noise coupling measurements.

SUMMARY

Substrate coupling and ground referencing problems are significantly affected by the substrate resistivity and the substrate and ground connection philosophies.

A mixed signal ASIC should have one "analog" ground reference plane for both the analog and digital circuits of the chip, and the digital transient current should be kept off of this plane.

While the standard conclusion may be that the substrate coupling situation is worse for chips with low resistivity substrates, this applies only to packaged chips which introduce impedance between chip and system grounds.

If an ASIC has a low resistivity substrate with an excellent quality backside contact, and is well connected directly to system ground, it exhibits close to ideal properties for isolation and referencing and can be used to great advantage:

-- Excellent isolation between circuits on different areas of the die (essentially no substrate coupling).

-- The substrate can be used as a low impedance ground current conduction path, eliminating some busses, bond pads, and bond wires, and improving performance.

-- Very low impedance referencing to one common ground for all analog circuits on the die.

-- Good latchup immunity can be provided by the backside contact exclusively.

Grounding and noise reduction is a far ranging subject which is very difficult to cover comprehensively. This paper attempts to clearly convey a few basic principles that were found essential in the design of the SVX3 chip. Hopefully it will be helpful to others involved in similar endeavors.